MEETING EMI REQUIREMENTS IN HIGH SPEED BOARD DESIGNS WITH ALLEGRO PCB SI

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Even though Signal Integrity (SI) is becoming more and more critical in today's high speed Printed Circuit Board (PCB) designs, electromagnetic interference (EMI) tests remain the only standard for an electronics product to go to market. This paper first presents the concept that good SI consideration on a high speed board design is essential in producing a board having the fewest EMI problems. It then discusses the tasks of enforcing EMI rules and the necessity of integrating automatic EMI rule checking into high speed PCB design flow. The paper finally presents the rule sets provided by EMControl, a module in Allegro PCB SI Expert, and how these rules can be automatically checked with the corresponding functionality..

I. INTRODUCTION

As signal speed transferred between chips and boards through packages goes up, it becomes more and more difficult for electronic products to pass EMI standard before going into market. Every component inside a product box has to be carefully designed to minimize EMI impact on the final system.

As the significant radiating component, high-speed PCBs need great attention to eliminate the causes that may fail EMI certification tests. Although there are many modern high-speed PCB analysis tools available to identify design problems, EMI effect remains as

the one that is almost impossible to be simulated in a complete and accurate fashion. To obtain accurate radiation effect, differential and common modes of emission have to be simulated for every net on board and the resulting electromagnetic fields in all directions need to be combined. Considering the large amount of nets (thousands of them, in many cases), it will take an un-realistically long time and require many trade-offs to reach a solution. And such trade-offs then sacrifice accuracy of results.

The fundamental objective of EMI engineers is to identify radiation sources and to eliminate them or make enclosure surrounding them. In practice, according to product requirements, EMI engineers define a set of design rules for board level designers to follow. The focus of the rules is to reduce radiation level and to prevent radiation damage by mechanical means. In modern high-speed PCB designs, however, the precautions suggested by EMI engineers become more and more difficult to comply with as PCBs become denser, which leaves little space for ground flooding or ground rings, etc… This means that radiation sources have to be eliminated if possible. It is clear now that proper SI consideration in high-speed designs is probably the best way to help achieve such a new EMI goal. With carefully minimizing reflections, crosstalk, and power delivery noises, SI requirements and considerations provide designers the possibility to get rid of high frequency components of signals which radiate the most and cause EMI problems. Therefore, addressing SI problems in high-speed designs becomes even more critical and essential today. This paper discusses the relationship between EMI and SI rules in high speed PCB design. It also presents what EMI rules are needed in general, and how these rules can be automatically checked with EMControl in Allegro PCB SI.

II. SI VS. EMI RULES

SI problems on a high-speed digital board are caused by the interconnect effects at fast edge rates. As the speed of signals on boards goes up, high frequency components from mis-managed SI problems, such as ringings, over/under-shoot, and coupling noise from neighboring signal traces, can convert into radiation energy and eventually fail the EMI test of a finished system. This explains why resolving SI problems on board can be of great assistance in achieving a quiet board in an EMI test. In addition, because good SI practice in high-speed PCBs can eliminate some critical radiation sources, corresponding EMI precautions are not necessary. Thus, space is saved to allow more cost-effective designs.

Take for example a CMOS output driver driving a 5 inch microstrip line. Without termination, there are significant reflections which translate into higher noise level in the frequency domain, as shown as the green trace in Figure 1. The frequency components of noise contribute greatly to emission level. This is why a group of un-terminated bus signals usually are identified as bad EMI source. In designs, SI engineers require terminators to be added in to avoid reflections. When the circuit we are discussing is terminated with a resistor whose value matches the trace impedance, the reflections are eliminated and the noise at frequency domain is reduced, shown as the black trace in Figure1.

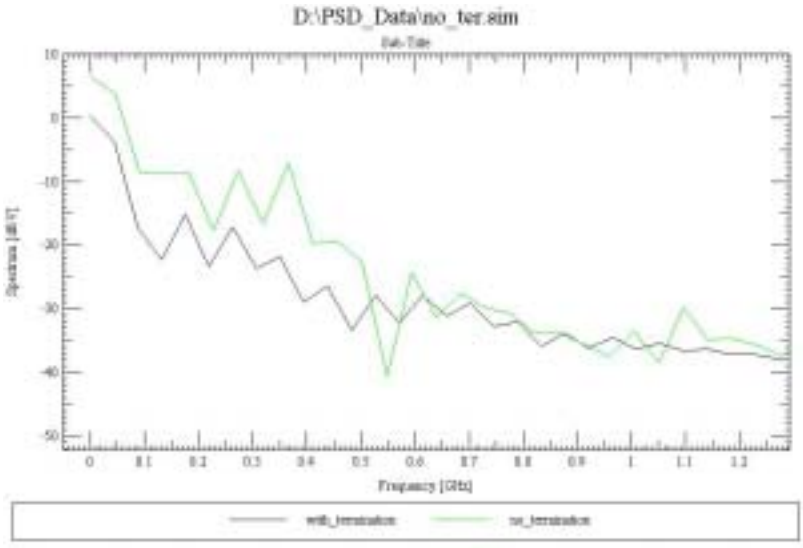


Figure 1 *Termination effect*

This example demonstrates how SI rules help eliminate emission causes in high-speed board designs.

In order to implement good SI considerations in a design, a set of SI rules have to be developed first and enforced during high-speed PCB designs to make sure that SI problems are avoided.

Allegro PCB SI provides users a way to develop optimum constraints (ECSets) and importantly a way to apply and track adherence to these constraints throughout the physical layout process. The same Constraint Manager that can be used within Allegro PCB SIduring floorplanning or critical signal what-if analysis can be used within Allegro (PCB Design Expert) to ensure that the design is being implemented as intended via the Electrical Constraint Sets. The application of rules within Allegro PCB SI or Allegro PCB Editor guarantees that critical signals are properly terminated, coupling noise from or to neighbor nets are minimized and appropriate decoupling capacitors are in place for ensuring reliable power supply to all components. With this kind of capability, Allegro PCB SI provides a complete constraint driven flow for designers and SI engineers to run simulations for both pre- and post-layout and to translate those pre-layout simulation results into electrical constraints. Many of these electrical constraints are SI oriented and EMI effective.

III. TASKS TO BE PERFORMED TO ENFORCE EMI RULES – OVERVIEW OF AN IDEAL EMI CHECKING PROCESS

After SI rules are properly implemented, many potential EMI problems can be cured at no extra cost. However, SI rules cannot completely replace EMI rules. Typical EMI rules need to be developed and enforced once SI rules are in place. It is equally important to have correct rules automatically checked. With the increased complexity in modern high-speed PCB designs, manually checking EMI rules by experienced EMI engineers would create almost impossible to meet tight product development schedules and cost budgets. EMI rule enforcement involves EMC experts, design engineers, and layout designers. Every one of them has specific tasks to perform for verifying whether or not a design is EMC compliant.

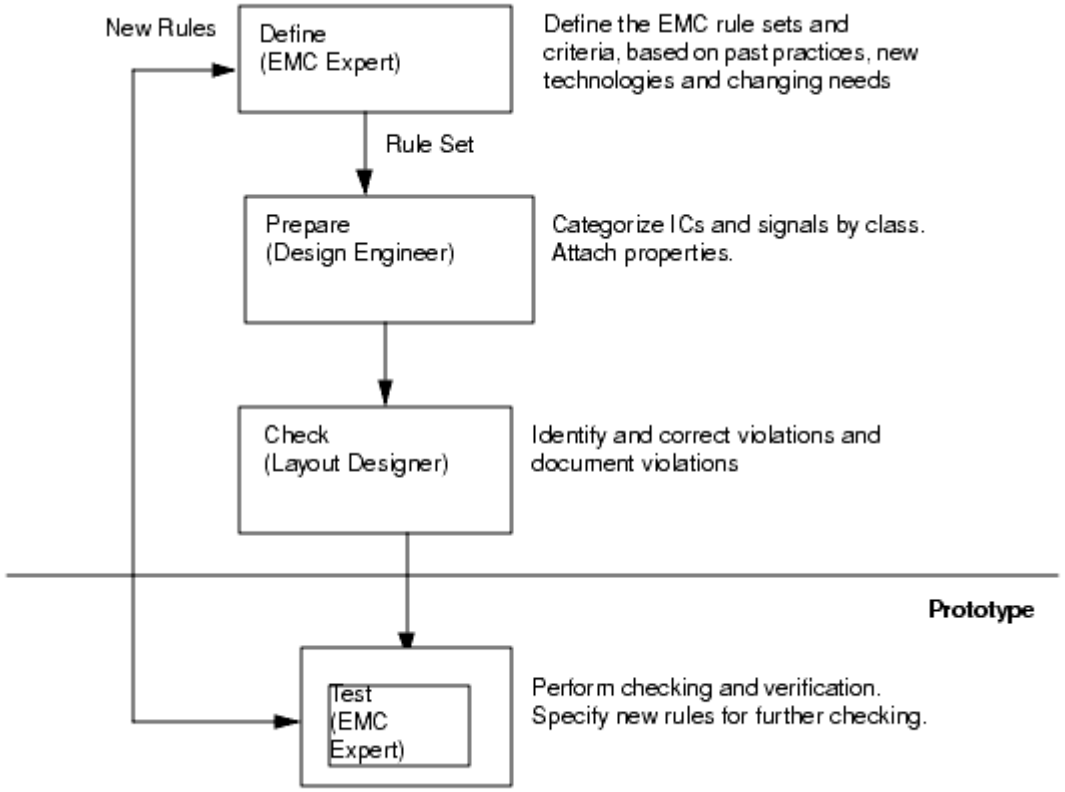


Figure 2 EMControl rule enforcement flow

First of all, EMC experts have to determine the EMC requirements for the design based on established EMC standards and engineering experience; to specify or develop project-specific, customized EMC rules and modify system-provided default EMC rules, if necessary; to select EMC rule sets for the different stages of design verification; and to review the results of EMC rule-checking runs and specify new EMC rule sets for further testing.

Secondly, design engineers will customize EMC rule variables (parameters) where required; assign relevant tool related properties to components and set the initial property values; set up the EMC rule-checking environment; specify the set of EMC rules to use during

each rule-checking run; specify the portion of the design to check for each rule set; and check the EMI rule checking tool setup and design preparation.

Thirdly, layout designers will run EMI rule checking; view EMC rule violation messages and correct problems in the design; and confer with the design engineer and the EMC expert as required while resolving violations.

Figure 2 shows this task flow.

IV. CHECKING EMI RULES WITH EMCONTROL IN Allegro PCB SI - OVERVIEW OF EMCONTROL

The objective of an EMI rule checker is to find EMI problems during designs. Some of these problems can be easily identified, which Allegro DRC rule sets are able to check. However, some of these problems are too complicated to be simulated or too time consuming to be identified by human. EMControl in Allegro PCB SI was designed for such applications. The newly enhanced EMControl provides users with two sets of rules to best meet EMI requirements. The Standard rule set aims to check general EMI problems that most designs need to avoid. The Advanced rule set contains many customized rules that are more application specific. Considering that EMI requirements vary from products to products, EMControl rule checker also provides users with an environment and means to develop and implement user defined rules. Figure 3 shows the rule set combination provided by EMControl in Allegro PCB SI.

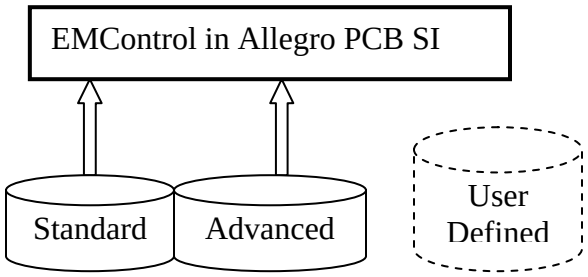


Figure 3 Rules in EMControl

The Standard rule set includes rules to check the density and locations of bypass capacitors, to identify and isolate noise components, to ensure proper termination, and to avoid routing problems of critical signals, such as signals too close to any reference plane edges or high speed signals on outer layers.

The Advanced rule set includes rules to shield critical signal nets, to limit decoupling capacitor leads, to minimize inductance loops on power delivery path, to check return current path of critical signals and to provide such paths with continuous reference planes, stitching capacitors, and ground vias.

EMControl rule checker, part of Allegro PCB SI Expert, can be launched from Allegro PCB Editor or Allegro PCB SI as Figure 4 shows. It enables the design engineer and the layout designer to perform the following tasks:

- Select specific EMC rule sets to check against the design, as shown in Figure 5.
- View a help file for each rule to determine:
- Whether or not the rule should be used for an EMC rule-checking run.
- Whether or not the rule should be customized.
- The properties and the property values required by the rule.
- The variables and their values required by the rule.
- Select the scope of the design that requires checking, as shown in Figure 6.
- Use Audit commands to verify that the properties required by the selected rules have been properly defined, as shown in Figure 7.
- Run the EMC rule checker to search for EMC violations.
- View the results of the check in a list of rule violations.
- Highlight an individual violation within the design, as shown in Figure 8.
- View the feedback from the Markers for correcting the EMC violations.

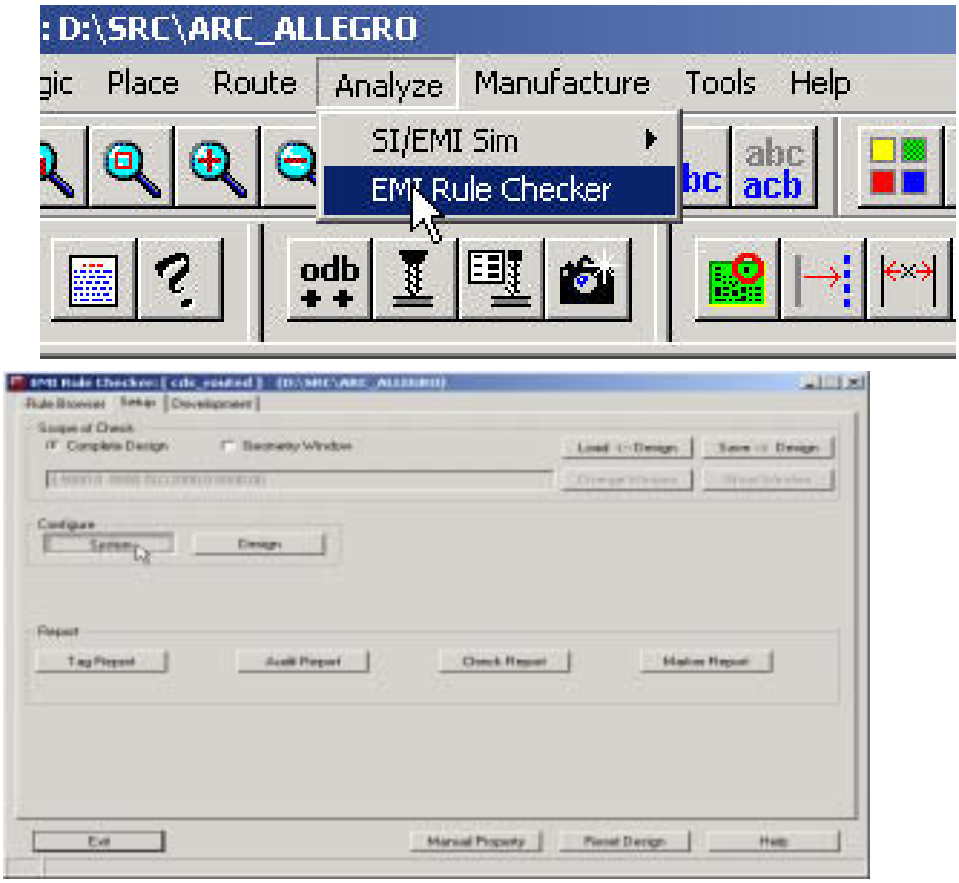


Figure 4 Access to EMControl, and EMControl user interface in Allegro PCB SI / Allegro PCB Editor

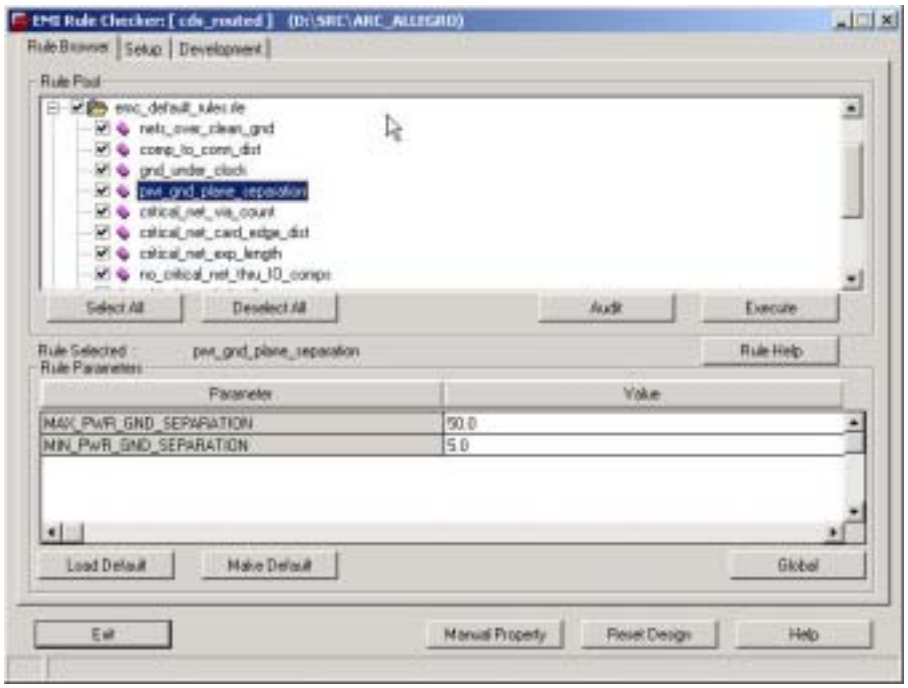


Figure 5 *Select specific EMC rule sets to check against the design*

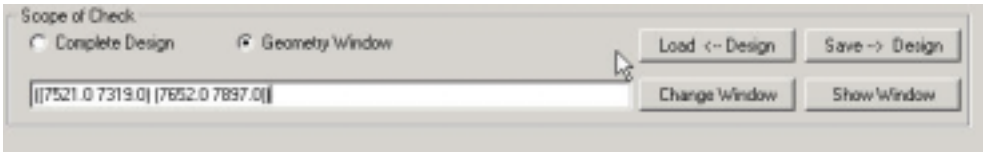


Figure 6 *Select the scope of the design that requires checking*

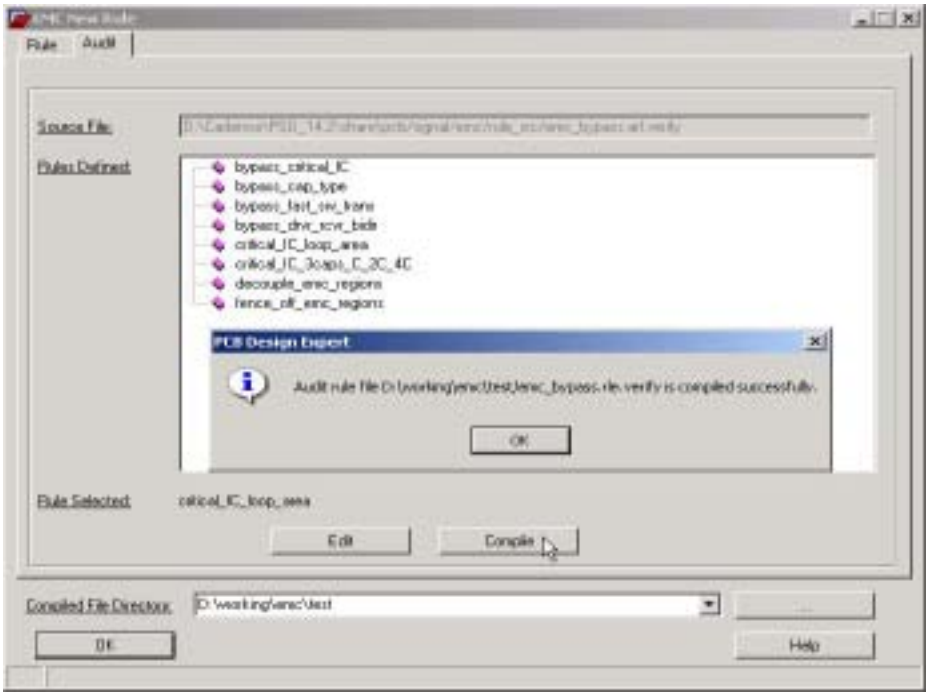


Figure 7 *Verify that the properties required by the selected rules have been properly defined*

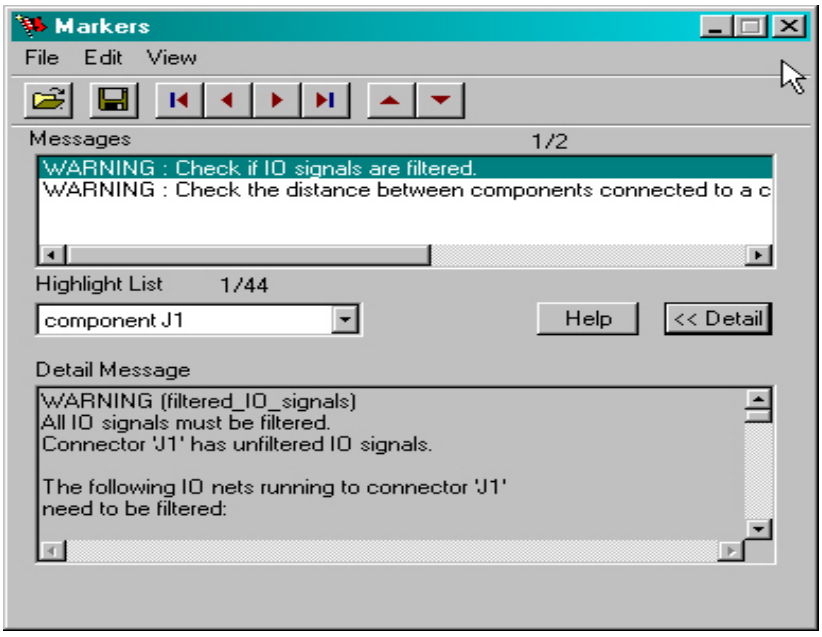
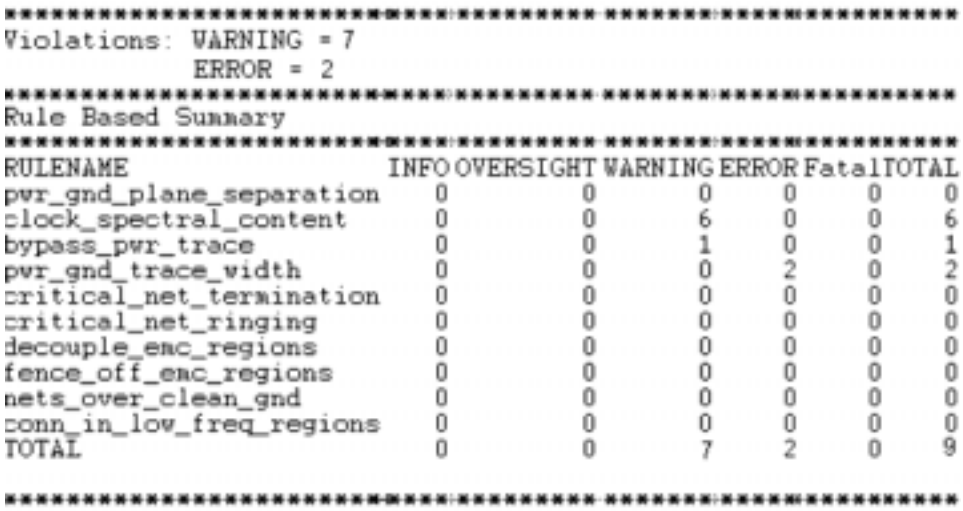


Figure 8 View violations within a design

An EMC expert can use EMControl to customize the default rule-checking in the following ways:

- Customizing default EMC rules locally by editing variable values
- Customizing default EMC rules for an entire site of users by editing variable values
- Writing and compiling new EMC rules, in the Cadence Advanced Rule Language (ARL).

EMControl can be used during the stages of placement (pre-route), routing, and post-route. The report from EMControl tells engineers EMI violations in design, as Figure 9 shows.



```
**************************************************************************
Violations: WARNING = 7
            ERROR = 2
**************************************************************************
Rule Based Summary
**************************************************************************
RULENAME                  INFO OVERSIGHT WARNING ERROR Fatal TOTAL
pwr_gnd_plane_separation     0         0       0     0     0     0
clock_spectral_content       0         0       6     0     0     6
bypass_pwr_trace             0         0       1     0     0     1
pwr_gnd_trace_width          0         0       0     2     0     2
critical_net_termination     0         0       0     0     0     0
critical_net_ringing         0         0       0     0     0     0
decouple_emc_regions         0         0       0     0     0     0
fence_off_emc_regions        0         0       0     0     0     0
nets_over_clean_gnd          0         0       0     0     0     0
conn_in_lov_freq_regions     0         0       0     0     0     0
TOTAL                        0         0       7     2     0     9

**************************************************************************
```

Figure 9 *EMControl Checking report*

V. USING RULES IN EMCONTROL - DETAILED EXAMPLE

The fundamental means of minimizing EMI problems are shielding, grounding, and providing continuous return current paths. EMControl rule checker includes the rules to satisfy these needs.

A critical issue customers are facing in today's designs is to ensure return current paths and to manage them effectively. Guaranteeing return current paths of critical signals is a complicated problem, which requires proper placement of decoupling capacitors and ground vias, and continuous signal reference planes. There have not been effective methods reported so far to explore and simulate the problem at an early design stage. The best approach is to identify the problem first. This requirement is now available within EMControl by the rules of finding return current path discontinuity and the rules of enforcing a certain number of decoupling capacitors and ground vias at designated locations. EMControl rule checker presents users with an advanced rule to check return paths of critical signal nets. The rule not only finds the return path discontinuity in routing regions on the board, but also reports such discontinuity when a signal path goes through the BGA areas. Figures 10 to 12 show a true design example in which the broken return path is captured and highlighted by using the rule checking critical signal's return current path.

Designs sometimes cannot avoid routing signals over split planes. EMControl rule checker then gives another rule to make sure of the existence of bypassing capacitors on either side of the plane split.

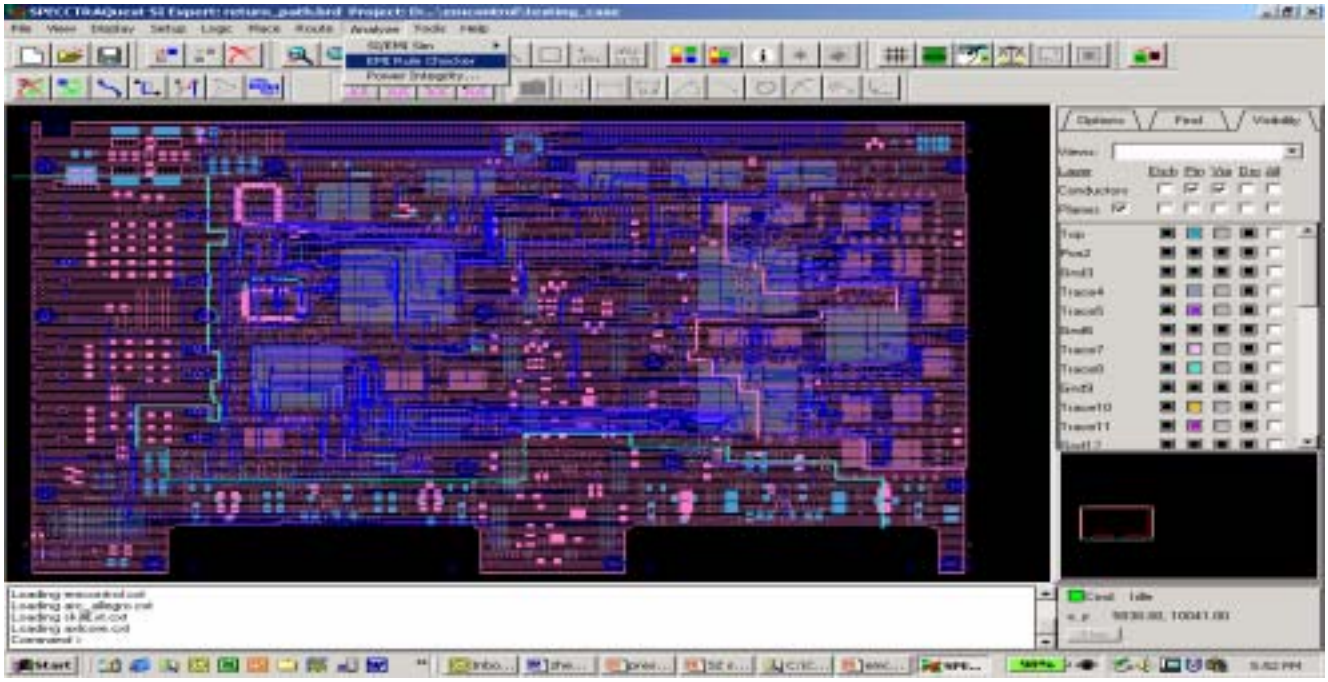


Figure 10. Design example – Finding return path problems

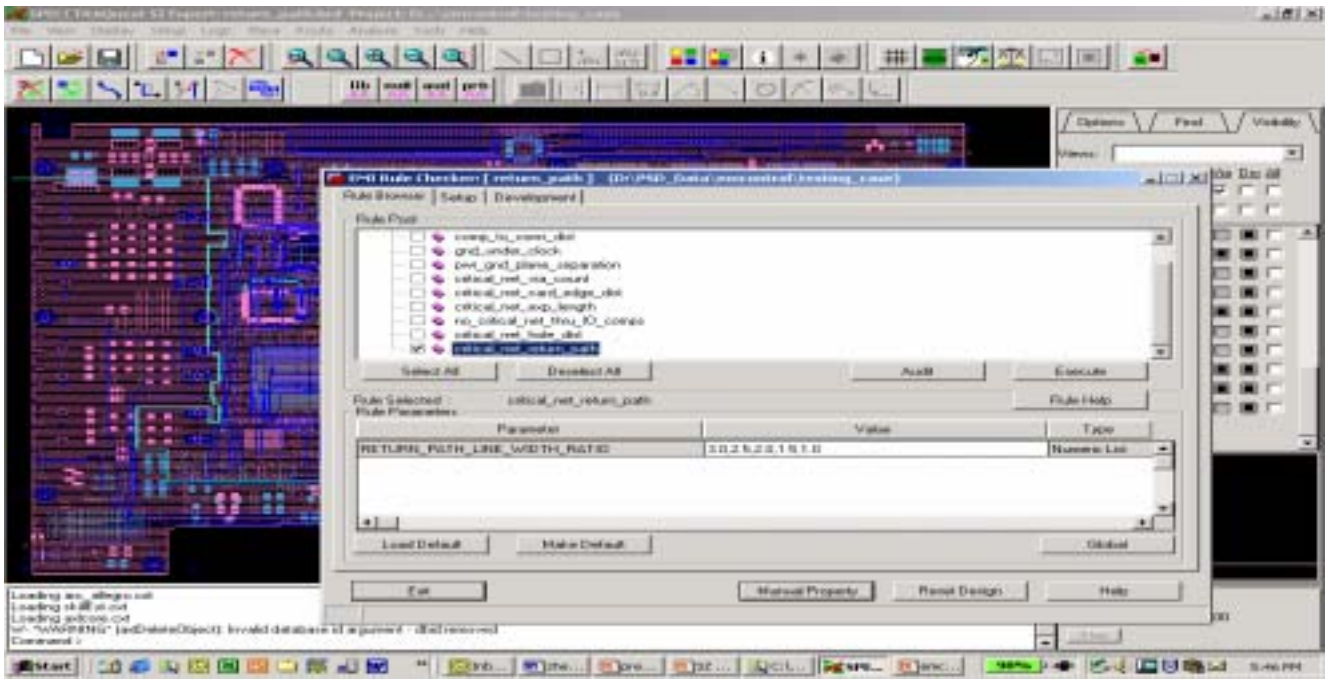


Figure 11. Design example – Using the rule of “critical_net_return_path

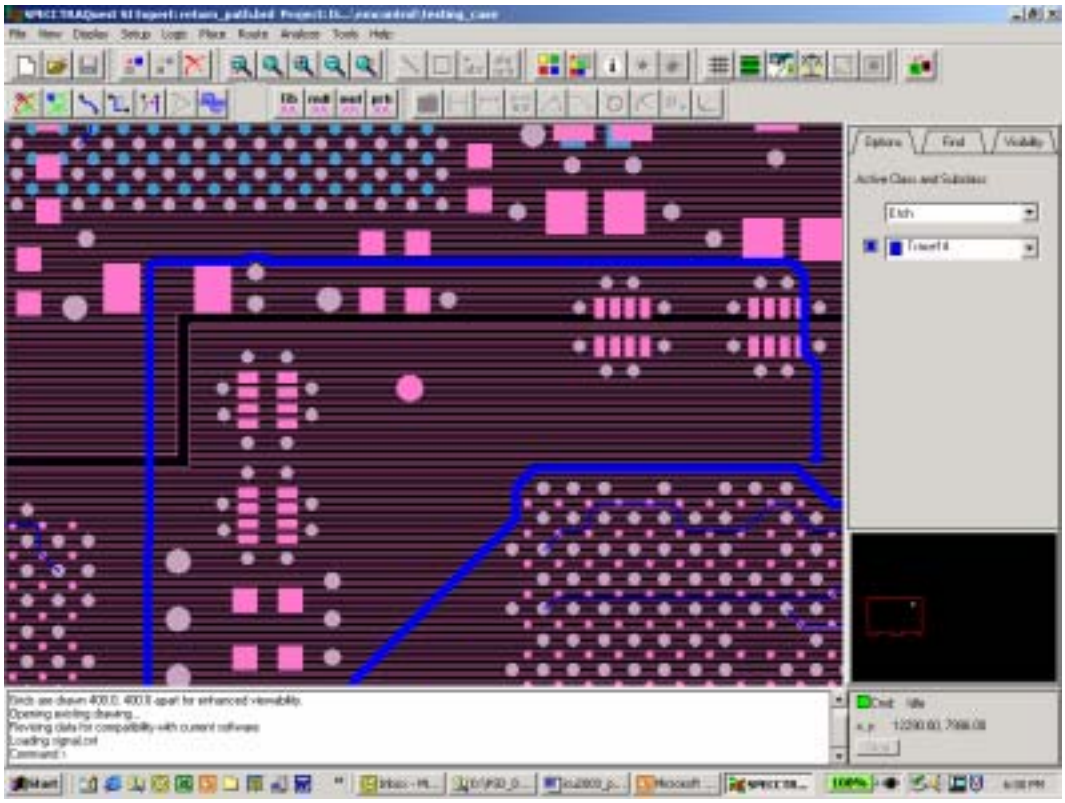


Figure 12 Design example - Signal crossing split planes is captured

VI.SUMMARY

Passing EMI tests is the key for an electronic product to go to market. Minimizing EMI impact caused by components of high-speed PCBs is essential for such success. This paper discusses how, in order to make a high-speed PCB with quiet EMI effects, both good SI considerations and EMI precautions must be implemented correctly during the design. To achieve this, corresponding SI and EMI rules need to be developed, enforced, and automatically examined. This paper then demonstrates how Allegro PCB SI as a high-speed PCB design tool, provides users with effective means, such as DRC, CM, and EMControl rule checker, to achieve such design goals.

VII. ACKNOWLEDGEMENT

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