

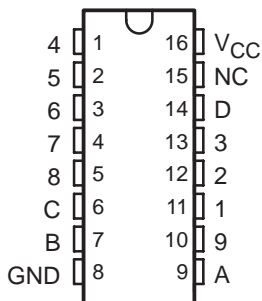
SN54147, SN54148, SN54LS147, SN54LS148 SN74147, SN74148 (TIM9907), SN74LS147, SN74LS148 10-LINE TO 4-LINE AND 8-LINE TO 3-LINE PRIORITY ENCODERS

SDLS053B – OCTOBER 1976 – REVISED MAY 2004

'147, 'LS147

- Encode 10-Line Decimal to 4-Line BCD
- Applications Include:
 - Keyboard Encoding
 - Range Selection

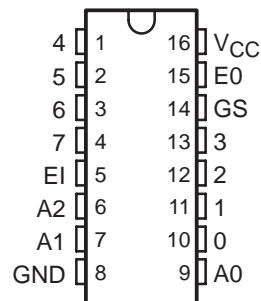
SN54147, SN54LS147 ... J OR W PACKAGE
SN74147, SN74LS147 ... D OR N PACKAGE
(TOP VIEW)



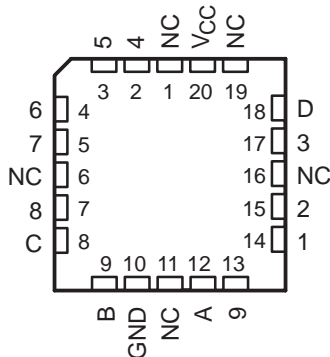
'148, 'LS148

- Encode 8 Data Lines to 3-Line Binary (Octal)
- Applications Include:
 - n-Bit Encoding
 - Code Converters and Generators

SN54148, SN54LS148 ... J OR W PACKAGE
SN74148, SN74LS148 ... D, N, OR NS PACKAGE
(TOP VIEW)

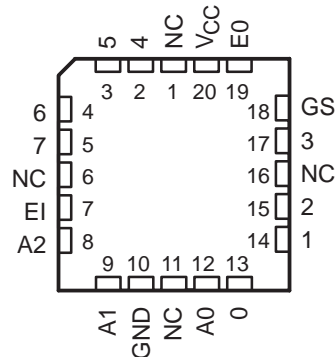


SN54LS147 ... FK PACKAGE
(TOP VIEW)



NC – No internal connection

SN54LS148 ... FK PACKAGE
(TOP VIEW)



TYPE	TYPICAL DATA DELAY	TYPICAL POWER DISSIPATION
'147	10 ns	225 mW
'148	10 ns	190 mW
'LS147	15 ns	60 mW
'LS148	15 ns	60 mW

NOTE: The SN54147, SN54LS147, SN54148, SN74147, SN74LS147, and SN74148 are obsolete and are no longer supplied.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2004, Texas Instruments Incorporated
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54147, SN54148, SN54LS147, SN54LS148
SN74147, SN74148 (TIM9907), SN74LS147, SN74LS148
10-LINE TO 4-LINE AND 8-LINE TO 3-LINE PRIORITY ENCODERS

SDLS053B – OCTOBER 1976 – REVISED MAY 2004

description/ordering information

These TTL encoders feature priority decoding of the inputs to ensure that only the highest-order data line is encoded. The '147 and 'LS147 devices encode nine data lines to four-line (8-4-2-1) BCD. The implied decimal zero condition requires no input condition, as zero is encoded when all nine data lines are at a high logic level. The '148 and 'LS148 devices encode eight data lines to three-line (4-2-1) binary (octal). Cascading circuitry (enable input EI and enable output EO) has been provided to allow octal expansion without the need for external circuitry. For all types, data inputs and outputs are active at the low logic level. All inputs are buffered to represent one normalized Series 54/74 or 54/74LS load, respectively.

ORDERING INFORMATION

T _A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74LS148N	SN74LS148N
	SOIC – D	Tube	SN74LS148D	LS148
		Tape and reel	SN74LS148DR	
	SOP – NS	Tape and reel	SN74LS148NSR	74LS148
–55°C to 125°C	CDIP – J	Tube	SNJ54LS148J	SNJ54LS148J
	CFP – W	Tube	SNJ54LS148W	SNJ54LS148W
	LCCC – FK	Tube	SNJ54LS148FK	SNJ54LS148FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE – '147, 'LS147

INPUTS									OUTPUTS			
1	2	3	4	5	6	7	8	9	D	C	B	A
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	L	H	H	H	H	H	L	L	H
X	X	X	L	H	H	H	H	H	H	L	H	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

H = high logic level, L = low logic level, X = irrelevant



SN54147, SN54148, SN54LS147, SN54LS148
SN74147, SN74148 (TIM9907), SN74LS147, SN74LS148
10-LINE TO 4-LINE AND 8-LINE TO 3-LINE PRIORITY ENCODERS

SDLS053B – OCTOBER 1976 – REVISED MAY 2004

FUNCTION TABLE – '148, 'LS148

INPUTS									OUTPUTS				
EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

H = high logic level, L = low logic level, X = irrelevant

**SN54147, SN54148, SN54LS147, SN54LS148
 SN74147, SN74148 (TIM9907), SN74LS147, SN74LS148
 10-LINE TO 4-LINE AND 8-LINE TO 3-LINE PRIORITY ENCODERS**

SDLS053B - OCTOBER 1976 - REVISED MAY 2004

'147, 'LS147 logic diagram (positive logic)



Pin numbers shown are for D, J, N, and W packages.

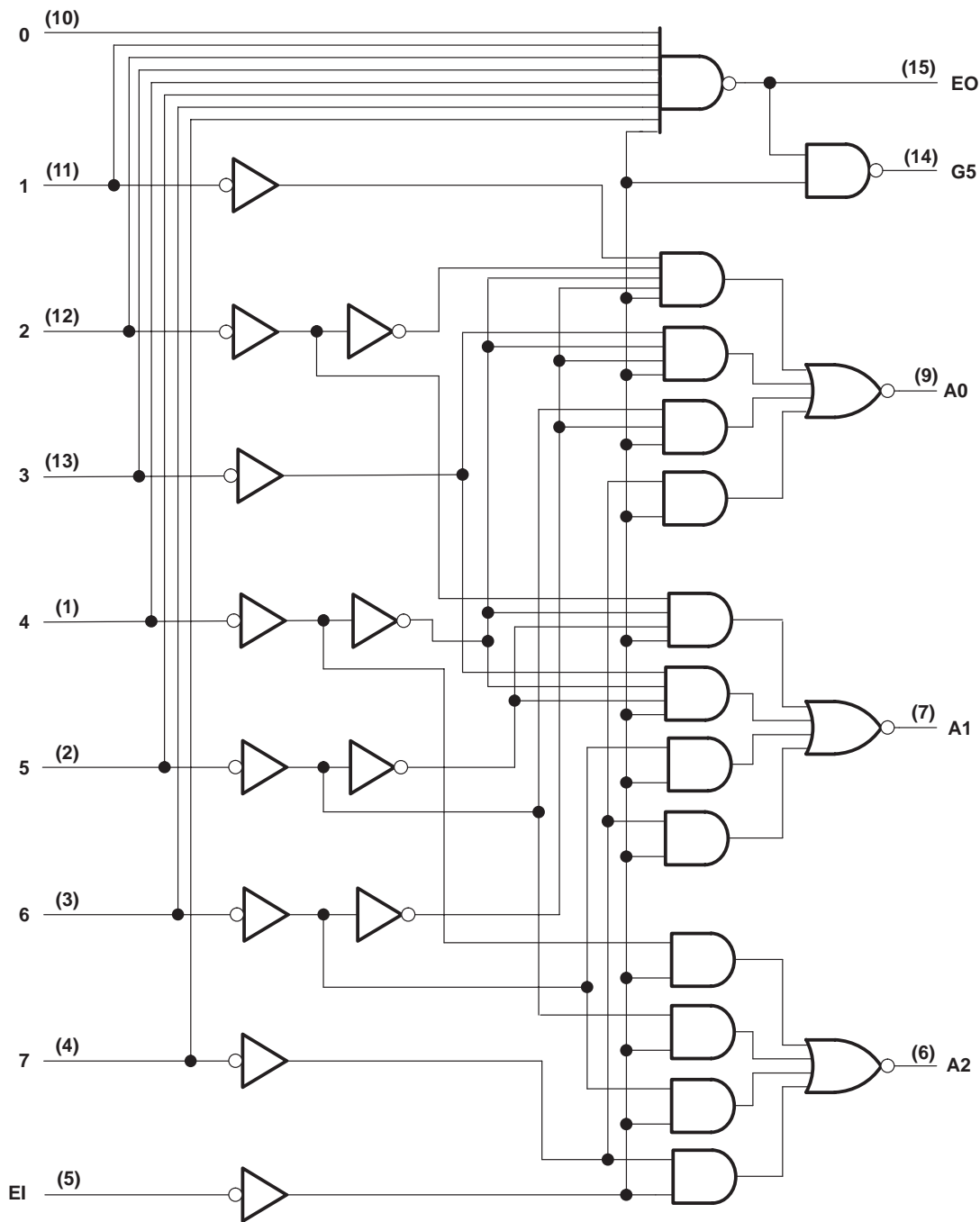


POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

**SN54147, SN54148, SN54LS147, SN54LS148
SN74147, SN74148 (TIM9907), SN74LS147, SN74LS148
10-LINE TO 4-LINE AND 8-LINE TO 3-LINE PRIORITY ENCODERS**

SDLS053B - OCTOBER 1976 - REVISED MAY 2004

'148, 'LS148 logic diagram (positive logic)



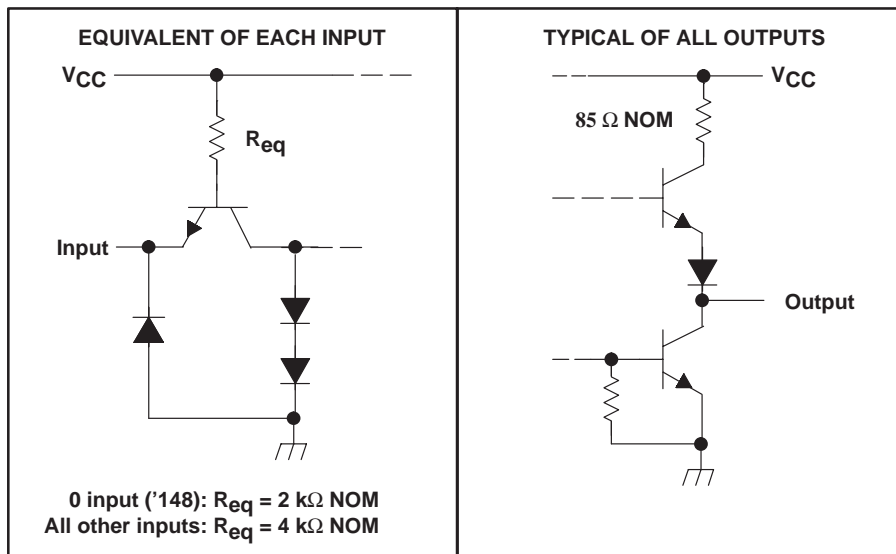
Pin numbers shown are for D, J, N, NS, and W packages.

**SN54147, SN54148, SN54LS147, SN54LS148
 SN74147, SN74148 (TIM9907), SN74LS147, SN74LS148
 10-LINE TO 4-LINE AND 8-LINE TO 3-LINE PRIORITY ENCODERS**

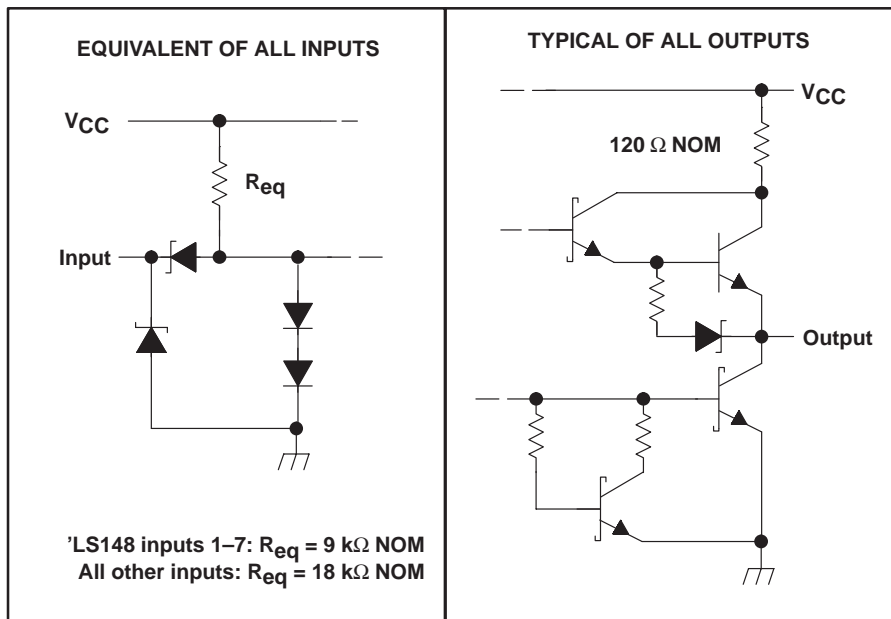
SDLS053B – OCTOBER 1976 – REVISED MAY 2004

schematics of inputs and outputs

'147, '148



'LS147, 'LS148



**SN54147, SN54148, SN54LS147, SN54LS148
SN74147, SN74148 (TIM9907), SN74LS147, SN74LS148
10-LINE TO 4-LINE AND 8-LINE TO 3-LINE PRIORITY ENCODERS**

SDLS053B – OCTOBER 1976 – REVISED MAY 2004

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage, V_I : '147, '148	5.5 V
'LS147, 'LS148	7 V
Inter-emitter voltage: '148 only (see Note 2)	5.5 V
Package thermal impedance θ_{JA} (see Note 3): D package	73°C/W
N package	67°C/W
NS package	64°C/W
Storage temperature range, T_{Stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. Voltage values, except inter-emitter voltage, are with respect to the network ground terminal.
 2. This is the voltage between two emitters of a multiple-emitter transistor. For '148 circuits, this rating applies between any two of the eight data lines, 0 through 7.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

	SN54'			SN74'			SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	4.5	5	5.5	4.75	5	5.25	V
I_{OH} High-level output current			–800			–800			–400			–400	μA
I_{OL} Low-level output current			16			16			4			8	mA
T_A Operating free-air temperature	–55		125	0		70	–55		125	0		70	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



**SN54147, SN54148, SN54LS147, SN54LS148
SN74147, SN74148 (TIM9907), SN74LS147, SN74LS148
10-LINE TO 4-LINE AND 8-LINE TO 3-LINE PRIORITY ENCODERS**

SDLS053B – OCTOBER 1976 – REVISED MAY 2004

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	'147			'148			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage				0.8			0.8	V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = -12 mA			-1.5			-1.5	V
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IL} = 0.8 V, V _{IH} = 2 V, I _{OH} = -800 μA	2.4	3.3		2.4	3.3		V
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IL} = 0.8 V, V _{IH} = 2 V, I _{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I _I	Input current at maximum input voltage	V _{CC} = MIN, V _I = 5.5 V			1			1	mA
I _{IH}	High-level input current	0 input						40	μA
		Any input except 0	V _{CC} = MAX, V _I = 2.4 V		40			80	
I _{IL}	Low-level input current	0 input						-1.6	mA
		Any input except 0	V _{CC} = MAX, V _I = 0.4 V		-1.6			-3.2	
I _{OS}	Short-circuit output current§	V _{CC} = MAX	-35		-85	-35		-85	mA
I _{CC}	Supply current	V _{CC} = MAX (See Note 5)	Condition 1	50	70	40	60		mA
			Condition 2	42	62	35	55		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

NOTE 5: For '147, I_{CC} (Condition 1) is measured with input 7 grounded, other inputs and outputs open; I_{CC} (Condition 2) is measured with all inputs and outputs open. For '148, I_{CC} (Condition 1) is measured with inputs 7 and EI grounded, other inputs and outputs open; I_{CC} (Condition 2) is measured with all inputs and outputs open.

SN54147, SN74147 switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	WAVEFORM	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	Any	Any	In-phase output	C _L = 15 pF, R _L = 400 Ω		9	14	ns
t _{PHL}						7	11	
t _{PLH}	Any	Any	Out-of-phase output			13	19	ns
t _{PHL}						12	19	



SN54147, SN54148, SN54LS147, SN54LS148
SN74147, SN74148 (TIM9907), SN74LS147, SN74LS148
10-LINE TO 4-LINE AND 8-LINE TO 3-LINE PRIORITY ENCODERS

SDLS053B – OCTOBER 1976 – REVISED MAY 2004

SN54148, SN74148 switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (see Figure 1)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	WAVEFORM	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	1–7	A0, A1, or A2	In-phase output	C _L = 15 pF, R _L = 400 Ω	10	15	ns	
t _{PHL}								
t _{PLH}	1–7	A0, A1, or A2	Out-of-phase output		12	19	ns	
t _{PHL}								6
t _{PLH}	0–7	EO	Out-of-phase output		14	25	ns	
t _{PHL}								18
t _{PLH}	0–7	GS	In-phase output		14	25	ns	
t _{PHL}								10
t _{PLH}	EI	A0, A1, or A2	In-phase output		10	15	ns	
t _{PHL}								8
t _{PLH}	EI	GS	In-phase output		10	15	ns	
t _{PHL}								10
t _{PLH}	EI	EO	In-phase output		10	15	ns	
t _{PHL}								17

† t_{PLH} = propagation delay time, low-to-high-level output.
t_{PHL} = propagation delay time, high-to-low-level output.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS'		SN74LS'		UNIT
			MIN	TYP‡	MAX	MIN	
V _{IH}	High-level input voltage		2		2		V
V _{IL}	Low-level input voltage					0.8	V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = -18 mA			-1.5		V
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IL} = 0.8 V, I _{OH} = -400 μA	2.5	3.4	2.7	3.4	V
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} MAX	I _{OL} = 4 mA		0.25	0.4	V
			I _{OL} = 8 mA			0.35	
I _I	Input current at maximum input voltage	'LS148 inputs 1–7	V _{CC} = MAX, V _I = 7 V		0.2		mA
		All other inputs			0.1		
I _{IH}	High-level input current	'LS148 inputs 1–7	V _{CC} = MAX, V _I = 2.7 V		40		μA
		All other inputs			20		
I _{IL}	Low-level input current	'LS148 inputs 1–7	V _{CC} = MAX, V _I = 0.4 V		-0.8		mA
		All other inputs			-0.4		
I _{OS}	Short-circuit output current§	V _{CC} = MAX	-20	-100	-20	-100	mA
I _{CC}	Supply current	V _{CC} = MAX (See Note 6)	Condition 1		12	20	mA
			Condition 2		10	17	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

NOTE 6: For 'LS147, I_{CC} (Condition 1) is measured with input 7 grounded, other inputs and outputs open; I_{CC} (Condition 2) is measured with all inputs and outputs open. For 'LS148, I_{CC} (Condition 1) is measured with inputs 7 and EI grounded, other inputs and outputs open; I_{CC} (Condition 2) is measured with all inputs and outputs open.



SN54147, SN54148, SN54LS147, SN54LS148
SN74147, SN74148 (TIM9907), SN74LS147, SN74LS148
10-LINE TO 4-LINE AND 8-LINE TO 3-LINE PRIORITY ENCODERS

SDLS053B – OCTOBER 1976 – REVISED MAY 2004

SN54LS147, SN74LS147 switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	WAVEFORM	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any	Any	In-phase output	$C_L = 15\text{ pF}$, $R_L = 2\text{ k}\Omega$	12	18	ns	
t_{PHL}					12	18		
t_{PLH}	Any	Any	Out-of-phase output		21	33	ns	
t_{PHL}					15	23		

SN54LS148, SN74LS148 switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (see Figure 2)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	WAVEFORM	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	1–7	A0, A1, or A2	In-phase output	$C_L = 15\text{ pF}$, $R_L = 2\text{ k}\Omega$	14	18	ns	
t_{PHL}					15	25		
t_{PLH}	1–7	A0, A1, or A2	Out-of-phase output		20	36	ns	
t_{PHL}					16	29		
t_{PLH}	0–7	EO	Out-of-phase output		7	18	ns	
t_{PHL}					25	40		
t_{PLH}	0–7	GS	In-phase output		35	55	ns	
t_{PHL}					9	21		
t_{PLH}	EI	A0, A1, or A2	In-phase output		16	25	ns	
t_{PHL}					12	25		
t_{PLH}	EI	GS	In-phase output		12	17	ns	
t_{PHL}					14	36		
t_{PLH}	EI	EO	In-phase output		12	21	ns	
t_{PHL}					23	35		

† t_{PLH} = propagation delay time, low-to-high-level output

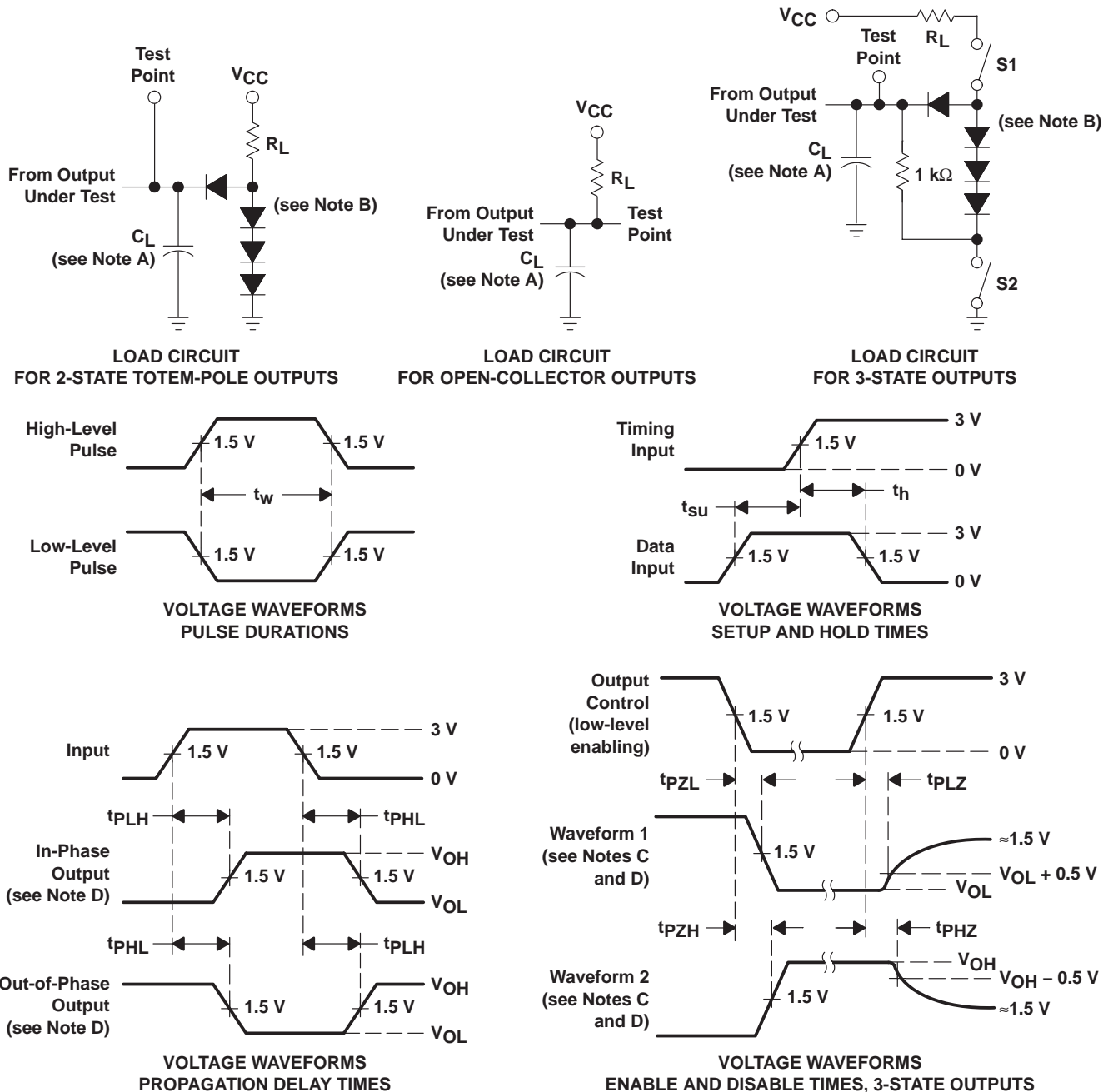
t_{PHL} = propagation delay time, high-to-low-level output



**SN54147, SN54148, SN54LS147, SN54LS148
SN74147, SN74148 (TIM9907), SN74LS147, SN74LS148
10-LINE TO 4-LINE AND 8-LINE TO 3-LINE PRIORITY ENCODERS**

SDLS053B – OCTOBER 1976 – REVISED MAY 2004

**PARAMETER MEASUREMENT INFORMATION
SERIES 54/74 DEVICES**



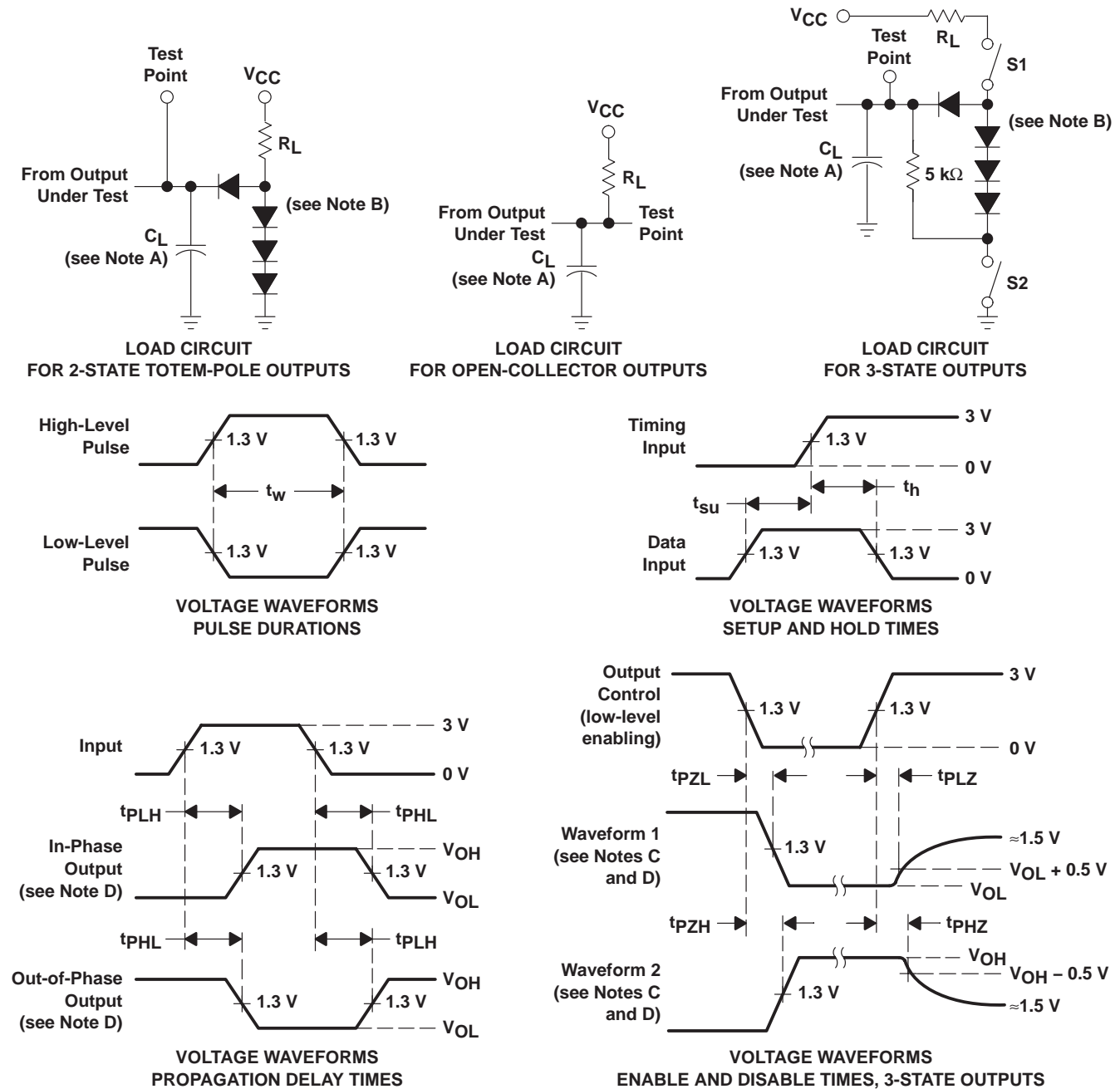
- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. All diodes are 1N3064 or equivalent.
 - C. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - D. S1 and S2 are closed for t_{PLH} , t_{PHL} , t_{PHZ} , and t_{PLZ} ; S1 is open, and S2 is closed for t_{PZH} ; S1 is closed, and S2 is open for t_{PZL} .
 - E. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_0 \approx 50 \Omega$; t_r and $t_f \leq 7$ ns for Series 54/74 devices and t_r and $t_f \leq 2.5$ ns for Series 54S/74S devices.
 - F. The outputs are measured one at a time, with one input transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

**SN54147, SN54148, SN54LS147, SN54LS148
SN74147, SN74148 (TIM9907), SN74LS147, SN74LS148
10-LINE TO 4-LINE AND 8-LINE TO 3-LINE PRIORITY ENCODERS**

SDLS053B – OCTOBER 1976 – REVISED MAY 2004

**PARAMETER MEASUREMENT INFORMATION
SERIES 54LS/74LS DEVICES**



- NOTES: A. C_L includes probe and jig capacitance.
 B. All diodes are 1N3064 or equivalent.
 C. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 D. S1 and S2 are closed for t_{PLH} , t_{PHL} , t_{PHZ} , and t_{PZL} ; S1 is open, and S2 is closed for t_{PZH} ; S1 is closed, and S2 is open for t_{PZL} .
 E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.
 F. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O \approx 50 \Omega$, $t_r \leq 1.5$ ns, $t_f \leq 2.6$ ns.
 G. The outputs are measured one at a time, with one input transition per measurement.

Figure 2. Load Circuits and Voltage Waveforms

**SN54147, SN54148, SN54LS147, SN54LS148
SN74147, SN74148 (TIM9907), SN74LS147, SN74LS148
10-LINE TO 4-LINE AND 8-LINE TO 3-LINE PRIORITY ENCODERS**

SDLS053B – OCTOBER 1976 – REVISED MAY 2004

APPLICATION INFORMATION

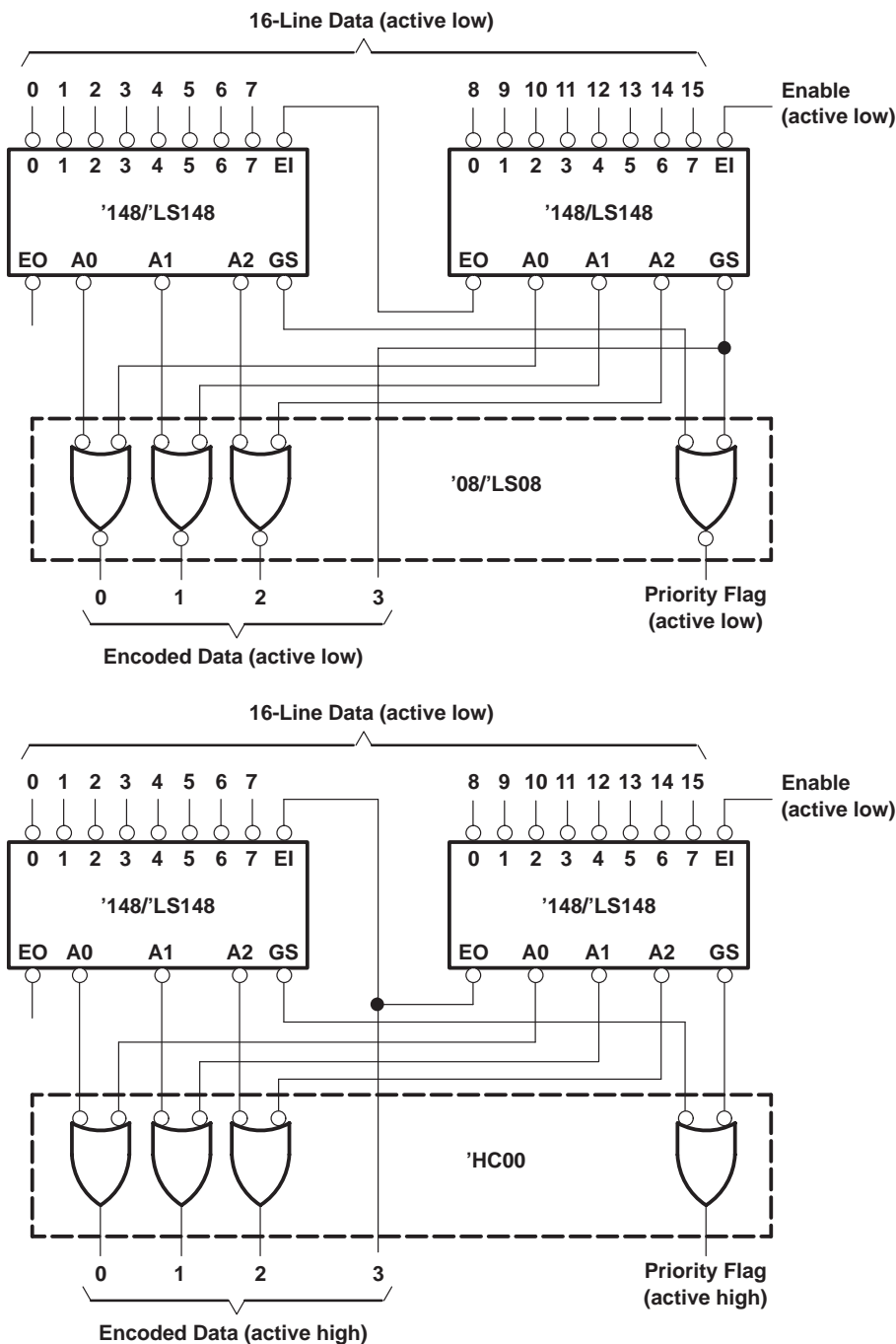


Figure 3. Priority Encoder for 16 Bits

Because the '147/LS147 and '148/LS148 devices are combinational logic circuits, wrong addresses can appear during input transients. Moreover, for the '148/LS148 devices, a change from high to low at EI can cause a transient low on GS when all inputs are high. This must be considered when strobing the outputs.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
78027012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
7802701EA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
7802701FA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
JM38510/36001B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
JM38510/36001BEA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
JM38510/36001BFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
SN54148J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SN54LS148J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SN74147N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74148J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SN74148N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74148N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74LS147DR	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
SN74LS147N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74LS148D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS148DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS148DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS148DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS148DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS148DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS148J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SN74LS148N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS148N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74LS148NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS148NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS148NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS148NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54148J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SNJ54148W	OBSOLETE	CFP	W	16		TBD	Call TI	Call TI
SNJ54LS148FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LS148J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS148W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

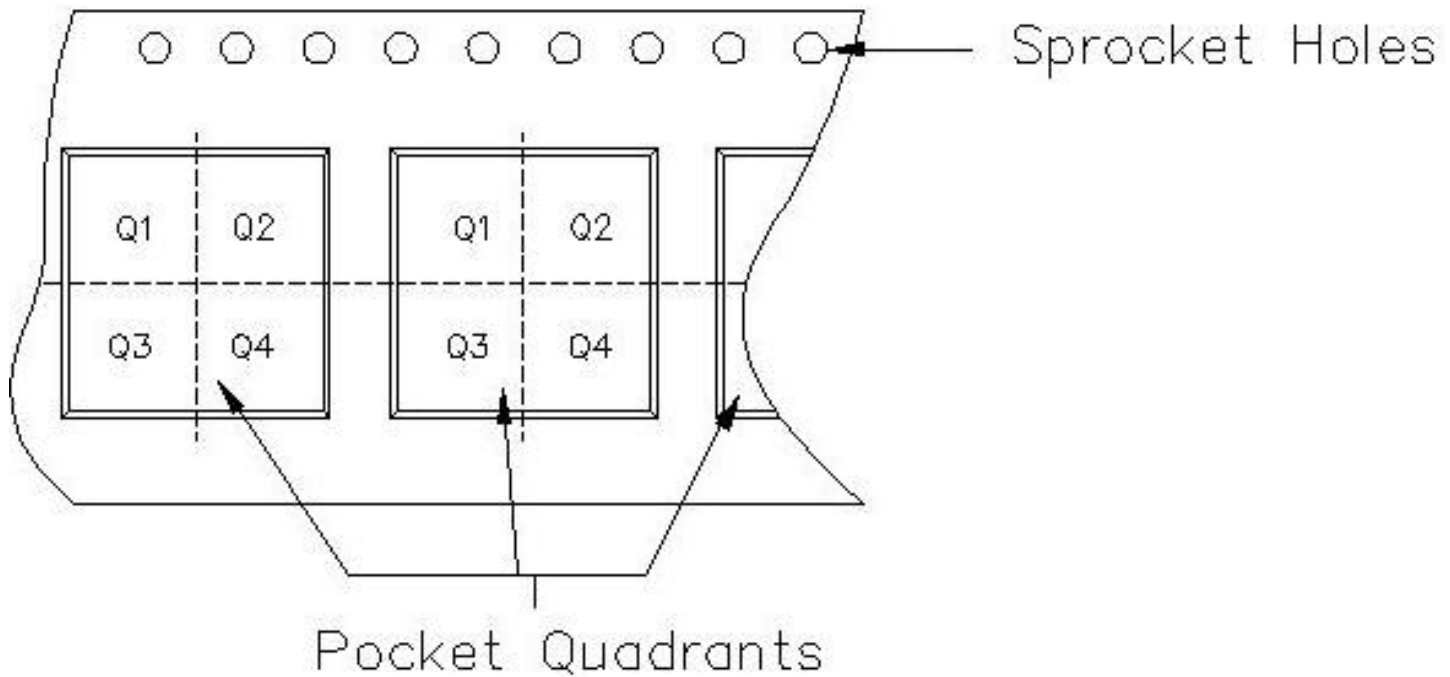
Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



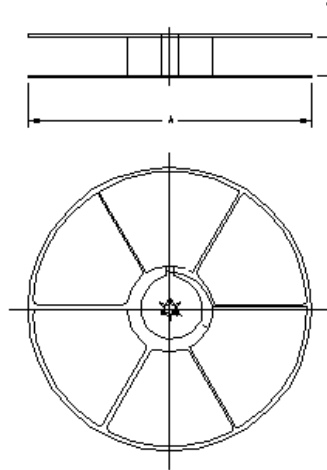
Carrier tape design is defined largely by the component length, width, and thickness.

A_o = Dimension designed to accommodate the component width.
B_o = Dimension designed to accommodate the component length.
K_o = Dimension designed to accommodate the component thickness.
W = Overall width of the carrier tape.
P = Pitch between successive cavity centers.



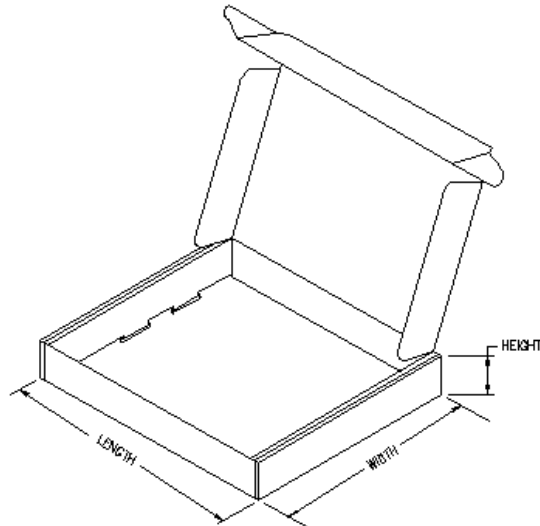
TAPE AND REEL INFORMATION

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS148DR	D	16	FMX	330	16	6.5	10.3	2.1	8	16	Q1
SN74LS148NSR	NS	16	MLA	330	16	8.2	10.5	2.5	12	16	Q1



TAPE AND REEL BOX INFORMATION

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
SN74LS148DR	D	16	FMX	342.9	336.6	28.58
SN74LS148NSR	NS	16	MLA	342.9	336.6	28.58



J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



4040140/D 10/96

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

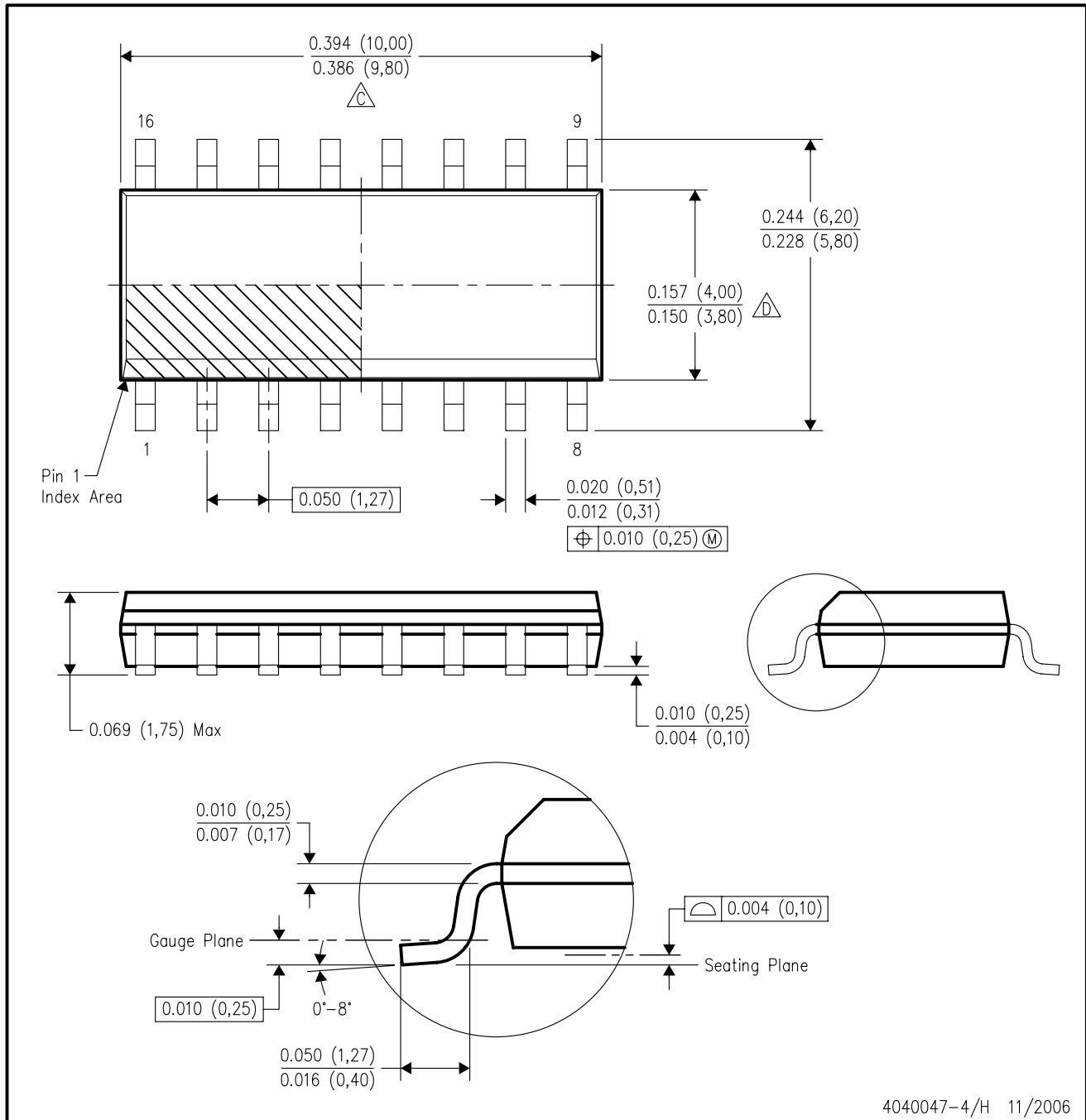
16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



4040047-4/H 11/2006

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AC.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Telephony	www.ti.com/telephony
Low Power Wireless	www.ti.com/lpw	Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2007, Texas Instruments Incorporated