AN EMBEDDED I_{DDQ} TESTING CIRCUIT AND TECHNIQUE*

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ABSTRACT

Quiescent current (I_{DDQ}) testing is a valuable defect detection technique in CMOS ICs. However, its application in very deep submicron technologies is susceptible to the increased transistor leakage current. In this paper, an I_{DDQ} testing technique and circuit are presented based on the background current compensation concept. This technique is independent from process and temperature variations and first experimental results from a fabricated circuit show that it is able to extend the viability of I_{DDQ} testing in future nanometer technologies.

1. INTRODUCTION

I_{DDQ} current testing is a powerful tool for the detection of defects in CMOS ICs. However, for present and future short channel, low threshold voltage technologies the effectiveness of I_{DDQ} testing is affected by technology scaling which leads to a remarkable increase of the intrinsic (defect-free) quiescent current (here after called background current, I_B) [1] while in parallel the defective currents are decreased [2]. The estimation is that the transistor leakage current is increased by a factor of 7.5 in every technology generation [3]. In addition, the number of transistors in a single chip is increased rapidly resulting in a further increase of I_B and a decrease in the gap between the values of I_B and any defective current (I_{DEF}). I_{DDQ} testing is also affected by the increased with technology evolution fluctuations in the value of the I_B due to manufacturing process variations. As a result, the application of I_{DDQ} testing may either lead to reduced fault coverage or yield loss.

A promising technique to overcome the above problems of I_{DDQ} testing was recently proposed in [4]. A Background Current Compensation (BCC) circuit is used, during testing, in order to compensate at the sensing node the expected background current I_B of the Circuit Under Test (CUT). An open question to that technique is how it will take into account the leakage current fluctuations due to manufacturing process as well as temperature variations. The adopted approach is to partition the CUT into two subcircuits. Then, the background current of the one subcircuit is used as reference for the generation of the compensation current for the other subcircuit and vice-versa. Since the reference currents are influenced by the same process and temperature variations in the CUT, the corresponding compensation currents are affected in a similar way by these factors. The current compensation circuit and technique presented in this paper target to provide a low cost and high resolution I_{DDQ} testing solution with high immunity to process and temperature variations.

The paper is organized as follows. In section 2 the proposed I_{DDQ} testing technique is presented while in section 3 design issues and experimental results, related to a fabricated demonstration circuit, are provided. Finally in section 4 the conclusions are drawn.

2. THE CURRENT COMPENSATION I_{DDQ} TESTING CONCEPT

In Fig. 1 the block schematic of the proposed technique is presented. The CUT is partitioned in two subcircuits (sub-CUT_L and sub-CUT_R). Then, the application of I_{DDQ} testing is divided in two successive phases. In the first phase where sub-CUT_L provides the reference current and sub-CUT_R is the circuit under test and the second phase where sub-CUT_R provides the reference current and sub-CUT_L is the circuit under test.

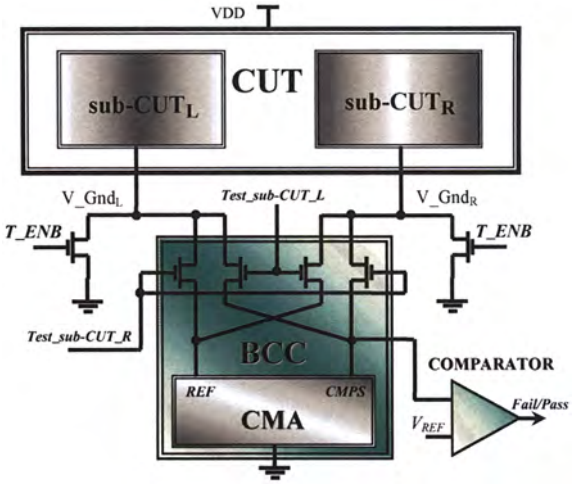

Figure 1. The proposed I_{DDQ} testing architecture

Each phase starts turning signal *T_ENB* to "low" and the corresponding *Test_sub-CUT_R* or *Test_sub-CUT_L* to "high" (see Fig. 2). A single Current Mirror Amplifier

* Partially funded by the structural funds of the Greek Ministry of Education within the framework of project "PYTHAGORAS"

(CMA) and a Comparator are used to test both subcircuits. In the first phase (*Test_sub-CUT_R* is "high" and *Test_sub-CUT_L* is "low") the background current I_{BL} of the sub-CUT_L, at the *REF* port of the CMA, is mirrored properly to its *CMPS* port and thus to the sensing node V_Gnd_R of the sub-CUT_R. This way a compensation current $I_{CMP\_R}=\beta_L I_{BL}=I_{BR}$ is generated that sinks the background current of sub-CUT_R. As a result, in the fault free case, the voltage on node V_Gnd_R drops below the reference voltage V_{REF} of the comparator. However, in the presence of a fault in sub-CUT_R the additional defective current raises the voltage at the sensing node V_Gnd_R above the V_{REF} voltage and the fault is detected. The phase ends turning *T_ENB* back to "high". In a similar way during the second phase (*Test_sub-CUT_R* is "high" and *Test_sub-CUT_L* is "low") the compensation current $I_{CMP\_L}=\beta_R I_{BR}=I_{BL}$ at the sensing node V_Gnd_L is generated in order to test sub-CUT_L. Note that β_L and β_R can take values lower than unity.

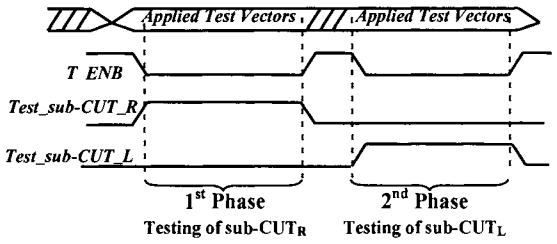

Figure 2. I_{DDQ} testing signals' waveforms

In Fig. 3 an effective ground supply partitioning technique is illustrated (similarly a V_{DD} supply partitioning scheme can be used) that provides equivalent dependence of both compensation currents on process and temperature variations by interdigitating inside the CUT two independent ground rails.

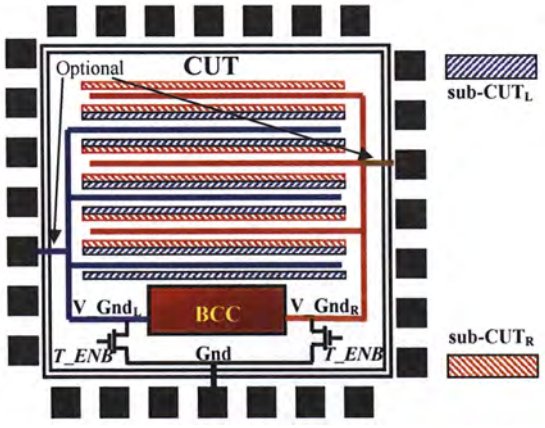

Figure 3. Possible supply partition technique (power rail)

However, the background current also depends on the applied test vector. In order to take into account this dependence a Programmable Current Mirror/Amplifier (PCMA) has been adopted for the implementation of the BCC circuit, that is a CMA with programmable current gain β. In that case simulations should be carried out in order to determine the required gain of the PCMA for each test vector of the test set applied to the CUT. This approach is applicable since the cardinality of an I_{DDQ} test set is very small [5]. Moreover, selecting suitably the proper test vectors, based on static power analysis [6-7], we can further reduce the background current variations from test vector to test vector. Then we can group together the test vectors for which the corresponding background currents present neighboring values keeping the size of the PCMA small. Possible differences between the simulated and the actual, in the field, background currents of the CUT do not invalidate the method since these variations affect in the same way both background currents.

3. I_{DDQ} TEST CHIP: EXPERIMENTAL RESULTS

3.1. The Demonstration circuit

In order to validate the proposed I_{DDQ} testing technique a demonstration circuit has been designed and fabricated in the standard 0.18μm CMOS technology of ST-Microelectronics (V_{DD}=1.8V). The demonstrator consists of a digital circuit, a PCMA circuit and a comparator that is used to discriminate defect free from defective cases. In addition a faulty cell constructed of two inverters with a 1KΩ resistance short circuit between their outputs is present. The faulty cell shares the same virtual ground (V_Gnd) with one subcircuit and can be properly activated by a *Fault_Enable* signal in order to insert a bridging fault in the circuit under test. However, it is possible to connect externally, between V_{DD} and V_Gnd nodes, any desired resistance value. The microphotograph of the demonstrator is shown in Fig. 4.

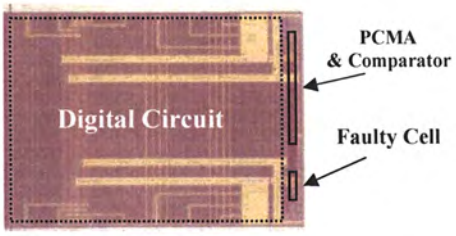

Figure 4. I_{DDQ} test chip microphotograph

A. The digital circuit: The digital circuit is the CUT. It is constructed of 10800 two input NAND and 10800 two input NOR gates. The circuit is partitioned into two subcircuits according to the ground supply partitioning technique of Fig 3. Each subcircuit contains half of the total circuit gates. For each subcircuit all its NAND gates are driven by a pair of signals and all its NOR gates are driven by another pair of signals. These eight signals in total are exploited to control the I_B of each subcircuit. This current ranges from about 100nA up to 10μA for all input combinations (256 combinations) in all process corners.

Although the size of the digital circuit is small to provide large background currents, this magnitude is not important in the validation of the proposed technique.

What is essential is the ability of this method to discriminate defect free from defective circuits when the background currents and the defective currents (to be detected) are comparable and a single voltage threshold is used.

B. The PCMA circuit: The design of the PCMA is shown in Fig. 5 and is based on the Wilson current mirror topology that has been selected due to its high output resistance [8]. It consists of six branches, three at the side of the reference port (*REF*) and three at the side of the compensation current generation port (*CMPS*). These mirrors act as current sinks at the virtual ground of the sub-$CUT_{R/L}$ under test in order to sink its background current $I_{B(R/L)}$. The reference current at the *REF* port of the PCMA is mirrored to its *CMPS* port and thus to the sensing node. Six select signals (SEL_1-SEL_6), one for each branch, are exploited to provide the programmability of the current mirror. These signals drive the select transistors MS1-MS6 and the corresponding full CMOS pass gates providing the ability to synthesize the proper compensation current for each test vector that is applied to the CUT.

PCMA and the other to a reference voltage V_{REF}=0.9V (see Fig. 1). The comparator has been designed so that its digital (fault indication) output *Fail/Pass* provides, during I_{DDQ} testing, a "high" response in case that a fault is present and a "low" response in the fault free case.

The required silicon area for the PCMA circuit and the comparator is only the 2.42% of the digital circuit under test. However, it is not necessary for the proposed technique any of these two circuits to be embedded with the CUT. This alternative approach may provide a higher flexibility in the design of these circuits. The only requirement is the proper partitioning of the CUT.

3.2. Experimental Results

According to the proposed I_{DDQ} testing technique, for every subcircuit and for every combination (test vector) at the inputs of the digital circuit a distinct activation vector <SEL_1-SEL_6> for the select signals has been determined through simulations in all process corners. This set of activation vectors has been used during the evaluation of the fabricated I_{DDQ} test chip (see Table I).

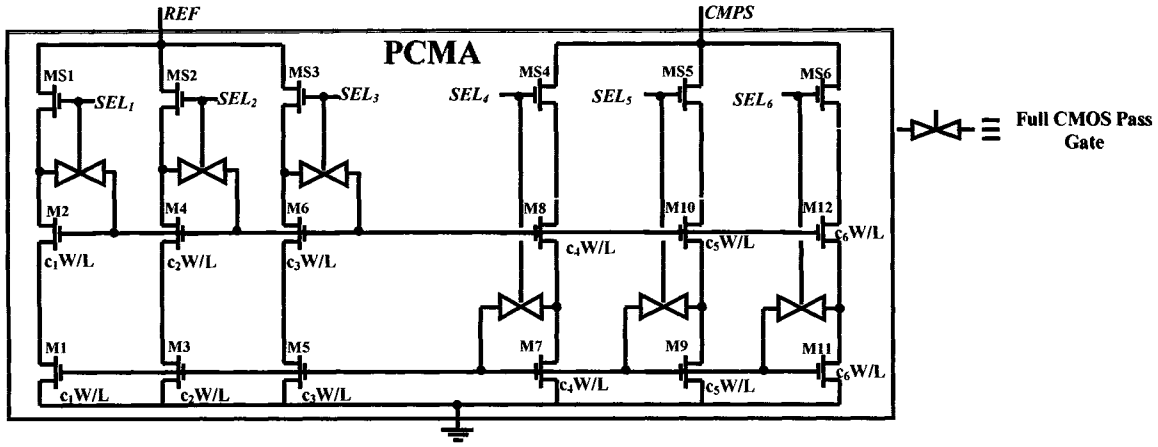

Figure 5. The used PCMA circuit

The widths of PCMA transistors used in the demonstration circuit are: i) for M_1, M_2 and MS_1 W=20μm, ii) for M_3, M_4 and MS_2 W=30μm, iii) for M_5, M_6 and MS_3 W=100μm, iv) for M_7, M_8 and MS_4 W=50μm, v) for M_9, M_{10} and MS_5 W=100μm and vi) for M_{11}, M_{12} and MS_6 W=200μm. These widths have been selected after electrical simulations for every input combination of the digital circuit, in every process corner of the used technology, and for temperatures from 25 to 85 ^{0}C, to generate all the required compensation currents. The length L of all transistors is 0.5μm. For the needs of a complete I_{DDQ} testing of the CUT, considering all input combinations in all possible process corners, only 10 states are required from a total of 49 PCMA programmable states.

C. The Comparator: The comparator is a simple differential amplifier that has been selected for its very high input resistance in order to avoid disturbing the compensation mechanism of the PCMA. One of the comparator's inputs is connected to the *CMPS* port of the

Table I - Test vector distribution per activation vector

Activation Vector <SEL_1-SEL_6>	Current Mirror Amplification Factor (β)	Number of Test Vectors
<100 – 010>	200/20	2
<100 – 110>	300/20	6
<010 – 100>	100/30	10
<010 – 010>	200/30	46
<010 – 110>	300/30	2
<001 – 001>	50/100	24
<001 – 100>	100/100	129
<001 – 101>	150/100	1
<001 – 010>	200/100	32
<001 – 110>	300/100	4
Total Test Vectors:		256

The evaluation procedure was as follows:

a) initially, the input vector is applied to the digital circuit while the virtual grounds ($V\_Gnd_{L/R}$) are

grounded (*T_ENB* is "high") and the PCMA and the faulty cell are inactive (fault free case – PCMA inactive);

b) then, the *T_ENB* is set to "low" and the I_{DDQ} test result is observed at the *Fail/Pass* port;
c) next, the *T_ENB* is set to "high" and the PCMA is activated applying the corresponding, predetermined activation vector (fault free case – PCMA active);
d) subsequently, the *T_ENB* is turned to "low" and the *Fail/Pass* signal is read,
e) next, the *T_ENB* is turned to "high" and the faulty cell is also activated (faulty case – PCMA active),
f) finally, the *T_ENB* is set to "low" and the *Fail/Pass* signal is observed.

This procedure has been followed for every possible input vector and the experimental results have shown that there is never an erroneous fault indication in the fault free case when the PCMA is active and that there is always a fault detection indication when a fault is present and the PCMA is active. This means that the proposed technique fulfills I_{DDQ} testing requirements without any loss either in the yield or the fault coverage. However, as it is illustrated in the logic analyzer view of Fig. 6 there were fault free cases, with the PCMA inactive (procedure steps a and b), where the result was an erroneous fault indication, which means that without the proposed technique these cases will lead to yield loss when a single discrimination threshold (V_{REF}) is used.

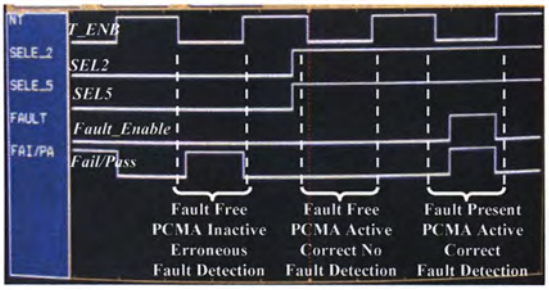

Figure 6. Experimental results from the fabricated chip

In order to characterize the I_{DDQ} test circuit and determine its resolution, external short circuit resistances with values up to 20MΩ (I_{DEF}=90nA) have been used. The measurements show that this circuit is capable to detect defective currents down to 3% of the circuit background current. Since the majority of defective resistances in a chip is up to 500Ω [9], then setting the desirable range of detectable defective resistances up to this value, which corresponds to a defective current up to 3.6mA (considering V_{DD}=1.8V), it is implied that with a 3% resolution the proposed design approach can be applied to circuits with background currents up to 0.12A. This is a very attractive result since it covers a wide range of circuit designs in this technology node. However, for higher background currents more partitions can be used.

4. CONCLUSIONS

In this work early experimental results on a new I_{DDQ} testing technique are presented. According to this technique, during I_{DDQ} testing, the background current at the sensing node of the CUT is compensated taking into account possible manufacturing process and temperature variations as well as the dependence of the background current on the applied test vector. This way any excessive defective current can be detected applying well known, simple, fast and high resolution sensing techniques using a single discrimination threshold. The adoption of this method is a promising solution to extend the viability of I_{DDQ} testing in future nanometer technologies.

5. ACKNOWLEDGMENT

The authors would like to thank Guillaume Prenat and Salvador Mir from TIMA Laboratory, Grenoble, France, for their suggestions and their support in the test chip fabrication.

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